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LMS7002M power supply connection

- Application note -

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1

Power pins and supply mode description

1.1 Overview

LMS7002M chip power supply pins can be separated into two groups:

1. Low voltage power supply pins. Supply line voltage – 1.25V and 1.4V;
2. High voltage power supply pins. Supply line voltage – 1.8V (optional additional 3.3V for digital input/output drivers).

LMS7002M power supply groups are shown in Figure 1. There are three groups (J5-K6; L5-K2; F8-D6) of pins that need external connections for the LMS7002M to work properly if internal low-dropout regulators (LDOs) are used. These pins are highlighted red in Figure 1. It should be noted, that four additional pin groups, in high (AH30-W33-W31; H32-T32) and low (AE29-AA29; R31-L33) voltage supply chains are connected internally. These pins are highlighted green in Figure 1.

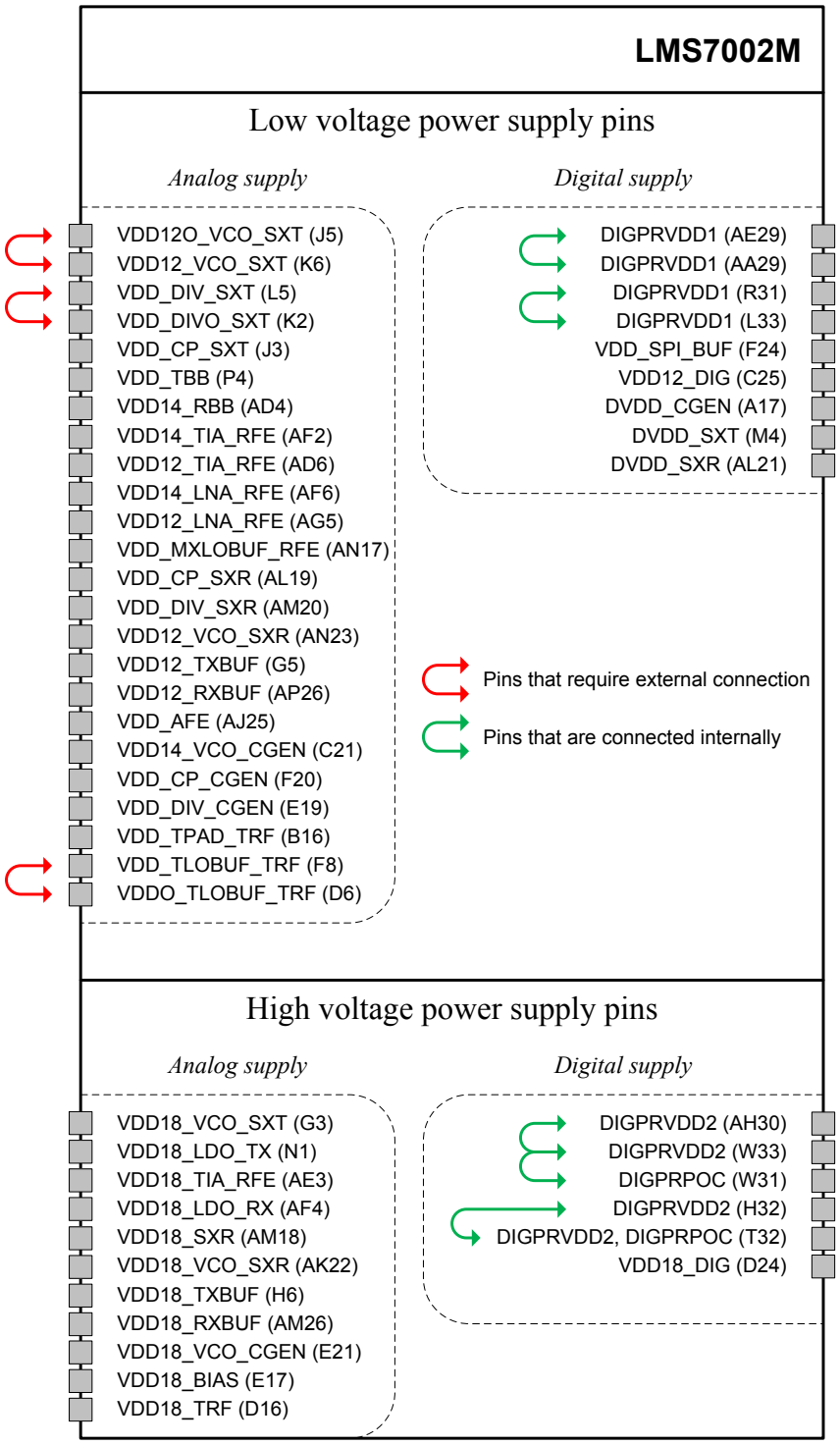

Figure 1. LMS7002M power supply pin diagram

1.2 Power pin description

A list of power supply pins and their description is given in Table 1.The pins are sorted by their appropriate connections to various analog and digital blocks.

Table 1: LMS7002M power pin description

Block	Pin ID	Pin Name	Supply type[A]	Supply voltage, V	Internal LDO?	Pin description
Transmitter (TX) synthesizer (SXR)	J5	VDD12O_VCO_SXT	A	1.25	Yes	SXT VCO LDO output
	K6	VDD12_VCO_SXT	A	1.25		Power supply for SXT VCO
	L5	VDD_DIV_SXT	A	1.25-1.4[B]	Yes	Power supply for SXT divider circuits
	K2	VDDO_DIV_SXT	A	1.25-1.4[B]		SXT divider circuit LDO output
	J3	VDD_CP_SXT	A	1.25	Yes	Power supply for SXT charge pump
	M4	DVDD_SXT	D	1.25	Yes	Power supply for SXT digital circuits
	G3	VDD18_VCO_SXT	A	1.8	No	Power supply for SXT VCO
TX radio frequency (RF) front-end (TRF)	B16	VDD_TPAD_TRF	A	1.25	Yes	Power supply for TRF power amplifier circuits
	F8	VDD_TLOBUF_TRF	A	1.25	Yes	Power supply for TRF RF path
	D6	VDDO_TLOBUF_TRF	A	1.25		TRF RF path circuit LDO output
	D16	VDD18_TRF	A	1.8	No	Power supply for TRF
TX analog base band (TBB)	P4	VDD_TBB	A	1.25	Yes	Power supply for TBB
TX clock buffer (TXBUF)	G5	VDD12_TXBUF	A	1.25	Yes	Power supply for TXBUF
	H6	VDD18_TXBUF	A	1.8-3.3[C]	No	Power supply for TXBUF
Receiver (RX) synthesizer (SXR)	AN23	VDD12_VCO_SXR	A	1.25	Yes	Power supply for SXR VCO
	AM20	VDD_DIV_SXR	A	1.25	Yes	Power supply for SXR divider circuits
	AL19	VDD_CP_SXR	A	1.25	Yes	Power supply for SXR charge pump
	AL21	DVDD_SXR	D	1.25	Yes	Power supply for SXR digital circuits
	AK22	VDD18_VCO_SXR	A	1.8	No	Power supply for SXR VCO
RX RF front-end (RFE)	AF6	VDD14_LNA_RFE	A	1.4	Yes	Power supply for RX LNA
	AG5	VDD12_LNA_RFE	A	1.25	Yes	Power supply for RX LNA
	AF2	VDD14_TIA_RFE	A	1.4	Yes	Power supply for RX TIA
	AD6	VDD12_TIA_RFE	A	1.25	Yes	Power supply for RX TIA and some RBB control blocks
	AN17	VDD_MXLOBUF_RFE	A	1.25-1.4[B]	Yes	Power supply for RX RF path circuits
RX analog base band (RBB)	AD4	VDD14_RBB	A	1.4	Yes	Power supply for RBB and ADC external input buffers
RX clock buffer (RXBUF)	AP26	VDD12_RXBUF	A	1.25	Yes	Power supply for RXBUF
	AM26	VDD18_RXBUF	A	1.8-3.3[C]	No	Power supply for RXBUF
Clock generator (CGEN)	C21	VDD14_VCO_CGEN	A	1.4	Yes	Power supply for CGEN VCO
	F20	VDD_CP_CGEN	A	1.25	Yes	Power supply for CGEN charge pump
	E19	VDD_DIV_CGEN	A	1.25	Yes	Power supply for CGEN divider circuits
	A17	DVDD_CGEN	D	1.25	Yes	Power supply for CGEN digital circuits
	E21	VDD18_VCO_CGEN	A	1.8	No	Power supply for CGEN VCO and CGEN internal LDOs
Analog front-end (AFE)	AJ25	VDD_AFE	A	1.25	Yes	Power supply for AFE (ADC and DAC)
BIAS	E17	VDD18_BIAS	A	1.8	No	Power supply for BIAS block
Serial port interface (SPI)	F24	VDD_SPI_BUF	D	1.25	Yes	Power supply for SPI core buffers
TX Transceiver Signal Processor (TSP)	AE29	DIGPRVDD1	D	1.25	Yes	Power supply for I/O pre-drivers, TX TSP, digital data and clock buffers
	AA29	DIGPRVDD1	D	1.25		
RX TSP	R31	DIGPRVDD1	D	1.25	Yes	Power supply for I/O pre-drivers, RX TSP, microcontroller (MCU), LimeLight™, SPI core
	L33	DIGPRVDD1	D	1.25		
Digital pad I/O drivers and power-on (POC) circuits	AH30	DIGPRVDD2	D	1.8-3.3[D]	No	Power supply for I/O post-drivers, POC circuits
	W33	DIGPRVDD2	D	1.8-3.3[D]		
	W31	DIGPRPOC	D	1.8-3.3[D]		
	H32	DIGPRVDD2	D	1.8-3.3[D]	No	
	T32	DIGPRVDD2, DIGPRPOC	D	1.8-3.3[D]		
Various	N1	VDD18_LDO_TX	A	1.8	No	Power supply for TBB, SXT, TRF LDO's, TBB external input switch control
	AE3	VDD18_TIA_RFE	A	1.8	No	Power supply for RFE, RBB, ADC external input buffers
	AF4	VDD18_LDO_RX	A	1.8	No	Power supply for RFE and RBB LDO's
	AM18	VDD18_SXR	A	1.8	No	Power supply for SXR and AFE LDOS's.
	C25	VDD12_DIG	A	1.25	Yes	Power supply for various digital circuits
	D24	VDD18_DIG	A	1.8	No	Power supply for various digital circuits

[A] – A= for analog circuits; D= for digital circuits

[B] – it is recommended to use 1.4 V for RF frequencies above 2.8 GHz

[C] – voltage level depends on the reference clock interface requirements.

[D] – voltage level depends on the I/O post-driver requirements. Datasheet specifications guaranteed only at 3.3 V

1.3 Supply option description

LMS7002M chip has two power supply options:

1. Multiple supply option – chip is powered by using several external power supply sources that generate 1.25V, 1.4V and 1.8V (optional 3.3V for digital input/output drivers);
2. Single supply option – chip is powered by using a single external 1.8V power source (optional 3.3V for digital input/output drivers).

As the name implies, multiple supply option uses several external supply power sources to generate the required voltage levels for the LMS7002M. The main disadvantage of this mode is the requirement for additional on-board components. Nonetheless, multiple supply option also provides several key advantages:

1. Higher efficiency regulators (for example, switched mode) can be used to reduce the overall power consumption of the system;
2. Maximum digital interface speeds that are given in the datasheet can only be reached by using external power supplies for the digital blocks of LMS7002M;

Single supply option uses a single 1.8V external power source – additional regulator can be used if digital pad driver I/O levels need to be of a different voltage. In this mode, all low voltage power supply pins generate their 1.25V and 1.4V supplies from the 1.8V power source using internal LDOs. A more detailed analysis of this option is presented in *Section 2.2*. Note, that the single power supply option is not suited for applications that might use the LMS7002M chip in Multiple-In-Multiple-Out (MIMO) configuration with full digital processing capabilities (see *Section 2.2*). Nonetheless, single supply option also provides several key advantages:

1. Dynamic low voltage power supply pin scaling for fine tuning and optimization;
2. Reduced Bill of Materials (BOM) cost and board size.

2

Supply pin connection

2.1 Connection to multiple external supply sources

Table 2 shows the power supply pin connection requirements and current consumption when all LMS7002M chip power supplies are generated on board from multiple power sources. Since some pins can be connected in several ways depending on multiple requirements, their connection options are given in a separate tab with default (recommended) values. Typical power pin grouping and LDO recommendations are shown in Figure 2.

Board related power supply connection guidelines and notes are presented in *Section 3*.

Table 2: LMS7002M pin connection to multiple external supply sources

Pin ID	Pin Name	Supply rail, V	Max current consumption, mA		Connection options
			Typical[A]	Maximum[B]	
J5	VDD12O_VCO_SXT	1.25		< 1	1. Connect to pin K6 (default) 2. Do not connect, leave floating
K6	VDD12_VCO_SXT	1.25	20	40	
L5	VDD_DIV_SXT	1.4	10	20	1. Connect to 1.4V rail for maximum RF performance (default) 2. Connect to 1.25V rail if RF frequency will not exceed 2.8GHz
K2	VDDO_DIV_SXT	1.4		< 1	1. Connect to pin L5 (default) 2. Do not connect, leave floating
J3	VDD_CP_SXT	1.25	3	10	
M4	DVDD_SXT	1.25	5	10	
G3	VDD18_VCO_SXT	1.8	30	80	
B16	VDD_TPAD_TRF	1.25	5	10	
F8	VDD_TLOBUF_TRF	1.25	90	120	
D6	VDDO_TLOBUF_TRF	1.25		< 1	1. Connect to pin F8 (default) 2. Do not connect, leave floating
D16	VDD18_TRF	1.8	20	80	
P4	VDD_TBB	1.25	30	80	
G5	VDD12_TXBUF	1.25	5	10	
H6	VDD18_TXBUF	1.8	2	10	1. Connect to 1.8V (default) 2. Connect to any other supply rail in the range of 1.8-3.3V according to the reference clock interface requirements
AN23	VDD12_VCO_SXR	1.25	20	40	
AM20	VDD_DIV_SXR	1.25	10	20	
AL19	VDD_CP_SXR	1.25	3	10	
AL21	DVDD_SXR	1.25	5	10	
AK22	VDD18_VCO_SXR	1.8	30	80	
AF6	VDD14_LNA_RFE	1.4	40	60	

Pin ID	Pin Name	Supply rail, V	Max current consumption, mA		Connection options
			Typical[A]	Maximum[B]	
AG5	VDD12_LNA_RFE	1.25	5	10	
AF2	VDD14_TIA_RFE	1.4	20	60	
AD6	VDD12_TIA_RFE	1.25	5	10	
AN17	VDD_MXLOBUF_RFE	1.4	140	180	1. Connect to 1.4V rail for maximum RF performance (default) 2. Connect to 1.25V rail if RF frequency will not exceed 2.8GHz
AD4	VDD14_RBB	1.4	40	80	
AP26	VDD12_RXBUF	1.25	5	10	
AM26	VDD18_RXBUF	1.8	2	10	1. Connect to 1.8V (default) 2. Connect to any other supply rail in the range of 1.8-3.3V according to the reference clock interface requirements
C21	VDD14_VCO_CGEN	1.4	5	10	
F20	VDD_CP_CGEN	1.25	3	5	
E19	VDD_DIV_CGEN	1.25	5	10	
A17	DVDD_CGEN	1.25	5	10	
E21	VDD18_VCO_CGEN	1.8	5	10	
AJ25	VDD_AFE	1.25	80	120	
E17	VDD18_BIAS	1.8	12	20	
F24	VDD_SPI_BUF	1.25	5	5	
AE29	DIGPRVDD1	1.25	100	400	
AA29	DIGPRVDD1	1.25			
R31	DIGPRVDD1	1.25	50	250	
L33	DIGPRVDD1	1.25			
AH30	DIGPRVDD2	3.3	20	120	1. Connect to 3.3V for maximum digital interface performance 2. Connect to any other supply rail in the range of 1.8-3.3V according to the digital interface requirements
W33	DIGPRVDD2	3.3			
W31	DIGPRPOC	3.3			
H32	DIGPRVDD2	3.3	20	120	
T32	DIGPRVDD2, DIGPRPOC	3.3			
N1	VDD18_LDO_TX	1.8	2	5	
AE3	VDD18_TIA_RFE	1.8	2	5	
AF4	VDD18_LDO_RX	1.8	2	5	
AM18	VDD18_SXR	1.8	2	5	
C25	VDD12_DIG	1.25	2	5	
D24	VDD18_DIG	1.8	2	5	

[A] – LMS7002M is configured in FDD MIMO mode, with 30.72MHz IF bandwidth and a carrier frequency that does not exceed 2.6GHz

[B] – conditional maximum pin current consumption

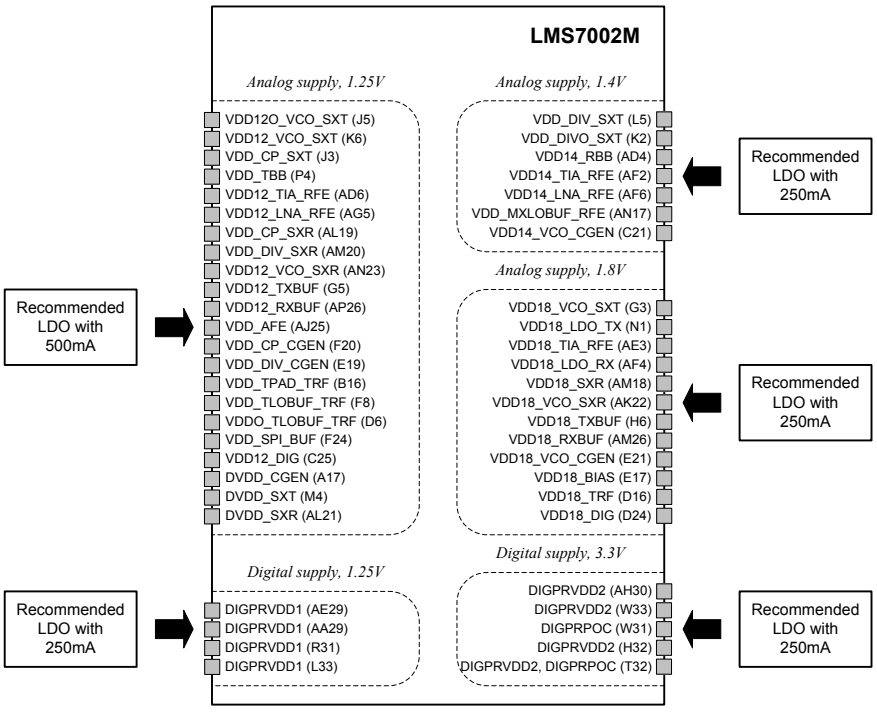

Figure 2. Recommended power pin grouping for typical LMS7002M power supply connection with multiple power sources

2.2 Connection to single external supply

When LMS7002M is used from a single power supply rail, several key features must be implemented in the designed board and in the software control:

1. Low voltage power pins (1.25V and 1.4V) should be connected to a 1μF capacitor that is connected to ground for stable internal LDO operation. Note, that for grouped pins, that require external connection to one another (see Figure 1), only one capacitor is needed per group;
2. CORE_LDO_EN (U33) pin needs to be tied to VDD (minimum 1.8V) or left unconnected (it has internal pull-up);
3. All internal LDO's need to be enabled. The required modifications for the Serial Peripheral Interface (SPI) memory map are listed in Table 3.

Table 3: Required modifications to the LMS7002M SPI for single external supply operation

Address	Bits	Setting
0x0092	[15:0]	1111 1111 1111 1111
0x0093	[15:0]	0000 0011 1111 1111
0x0099	[15:0]	0110 0101 1000 1100
0x009E	[15:0]	1000 1100 1000 1100

Table 4 shows the power supply pin connection requirements and current consumption when all LMS7002M chip power supplies are generated on board from a single 1.8V power source. Note, that digital interface power pins may need to be connected to a different power source according to the digital interface requirements. Typical power pin grouping and LDO recommendations are shown in Figure 3.

As noted in Section 1.3, single external supply is not recommended when the digital TSP blocks of LMS7002M are used at their full processing capabilities. Full digital block processing capabilities are considered enabled when the chip is running in MIMO configuration with every TSP sub-block enabled, while TxTSP and RxTSP are running at 640MHz and 160MHz respectively. Typical max current consumptions for digital pins are given with TxTSP and RxTSP General Purpose Finite Impulse Response (GFIR) filters bypassed.

Board related power supply connection guidelines and notes are presented in *Section 3*.

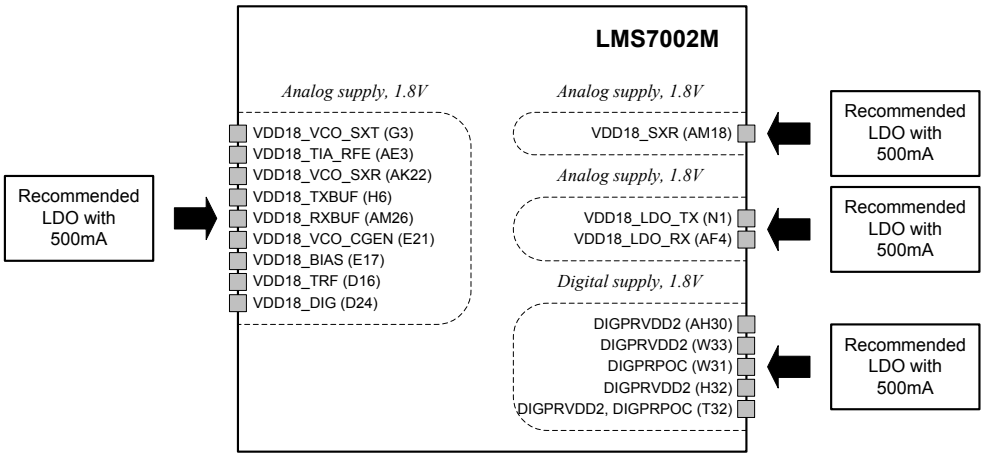

Figure 3. Recommended power pin grouping for typical LMS7002M power supply connection with a single power sources

Table 4: LMS7002M pin connection to a single external supply source

Pin ID	Pin Name	Supply rail, V	Max current consumption, mA		Connection options
			Typical[A]	Maximum[B]	
G3	VDD18_VCO_SXT	1.8	30	80	
D16	VDD18_TRF		20	80	
H6	VDD18_TXBUF		7	20	
AK22	VDD18_VCO_SXR		30	80	
AM26	VDD18_RXBUF		8	21	
E21	VDD18_VCO_CGEN		27	49	
E17	VDD18_BIAS		12	20	
AH30	DIGPRVDD2		120	525	1. Connect to 1.8V for single power supply option 2. Connect to 3.3V for maximum digital interface performance 3. Connect to any other supply rail in the range of 1.8-3.3V according to the digital interface requirements
W33	DIGPRVDD2				
W31	DIGPRPOC				
H32	DIGPRVDD2		70	375	
T32	DIGPRVDD2, DIGPRPOC				
N1	VDD18_LDO_TX		170	300	
AE3	VDD18_TIA_RFE		2	5	
AF4	VDD18_LDO_RX		115	225	
AM18	VDD18_SXR		265	390	
D24	VDD18_DIG		10	20	

[A] – LMS7002M is configured in FDD MIMO mode, with 30.72MHz IF bandwidth and a carrier frequency that does not exceed 2.6GHz

[B] – conditional maximum pin current consumption

3

Recommendations for board design

3.1 Power supply pin connection

There are three recommended power supply pin connection types to the external voltage regulators. The connections are shown in Figure 4. The pin list, with recommended connection option is given in Table 5.

If the chip is run from internal LDOs, only the capacitor(s) directly connected to the low voltage LMS7002M pins should be used. They are needed to guarantee stable internal LDO operation.

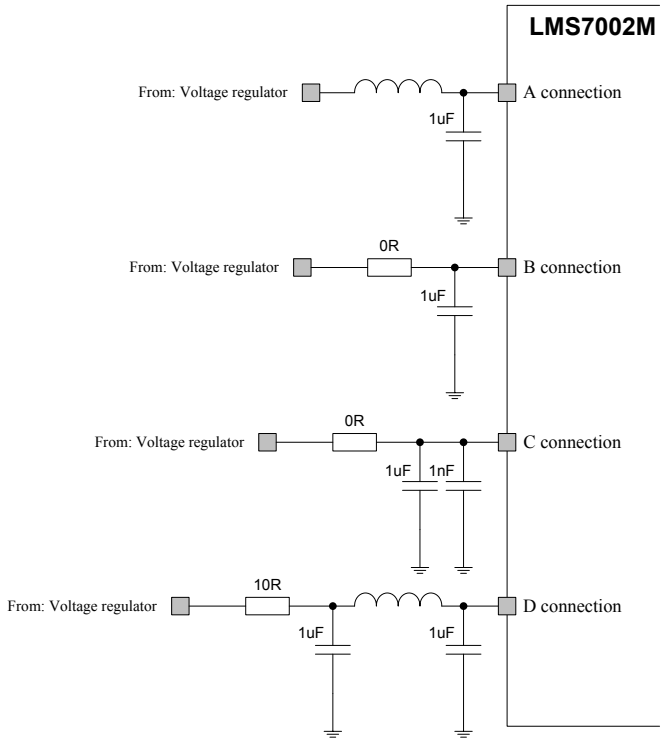

Figure 4. LMS7002M power pin connection to on-board LDOs options

Table 5: LMS7002M pin connection to multiple external supply sources

Pin ID	Pin Name	Connection option from Figure 4
J5	VDD12O_VCO_SXT	A
K6	VDD12_VCO_SXT	
L5	VDD_DIV_SXT	A
K2	VDDO_DIV_SXT	
J3	VDD_CP_SXT	B
M4	DVDD_SXT	A
G3	VDD18_VCO_SXT	A
B16	VDD_TPAD_TRF	A
F8	VDD_TLOBUF_TRF	A
D6	VDDO_TLOBUF_TRF	
D16	VDD18_TRF	A
P4	VDD_TBB	A
G5	VDD12_TXBUF	D
H6	VDD18_TXBUF	D
AN23	VDD12_VCO_SXR	A
AM20	VDD_DIV_SXR	A
AL19	VDD_CP_SXR	B
AL21	DVDD_SXR	A
AK22	VDD18_VCO_SXR	A
AF6	VDD14_LNA_RFE	A
AG5	VDD12_LNA_RFE	A
AF2	VDD14_TIA_RFE	A
AD6	VDD12_TIA_RFE	A
AN17	VDD_MXLOBUF_RFE	A
AD4	VDD14_RBB	A
AP26	VDD12_RXBUF	D
AM26	VDD18_RXBUF	D
C21	VDD14_VCO_CGEN	A
F20	VDD_CP_CGEN	B
E19	VDD_DIV_CGEN	A
A17	DVDD_CGEN	A
E21	VDD18_VCO_CGEN	A
AJ25	VDD_AFE	A
E17	VDD18_BIAS	A
F24	VDD_SPI_BUF	A
AE29	DIGPRVDD1	C
AA29	DIGPRVDD1	C
R31	DIGPRVDD1	C
L33	DIGPRVDD1	C
AH30	DIGPRVDD2	C
W33	DIGPRVDD2	C
W31	DIGPRPOC	C
H32	DIGPRVDD2	C
T32	DIGPRVDD2, DIGPRPOC	C
N1	VDD18_LDO_TX	A
AE3	VDD18_TIA_RFE	A
AF4	VDD18_LDO_RX	A
AM18	VDD18_SXR	A
C25	VDD12_DIG	A
D24	VDD18_DIG	A

When selecting and LDO's, keep attention to the power-supply rejection ratio (PSRR) and the output noise. The PSSR should be >60dB at 1kHz, while the output noise should be >0.25µV√Hz at 1KHz.

3.2 TX power amplifier supply connection

TX power amplifier (PA) is supplied from its output pins from a 1.8V source. A typical TX output connection is shown in Figure 5. The inductor and matching network values depend on desired output frequency. There are two power amplifier outputs per TX channel and only one can be working at a time. The maximum power supply requirement per channel is 100mA (MIMO mode 200mA), with a typical value close to 70mA (MIMO mode 140mA).

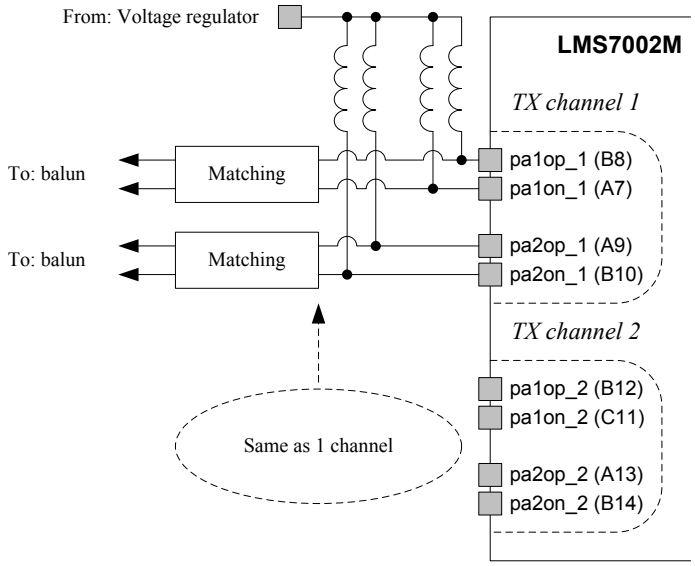

Figure 5. LMS7002M TX output connection